

A Low-Power Wideband CMOS LNA for WiMAX

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Abstract—In this brief, the design of a low-power inductorless wideband low-noise amplifier (LNA) for worldwide interoperability for microwave access covering the frequency range from 0.1 to 3.8 GHz using 0.13- μm CMOS is described. The core consumes 1.9 mW from a 1.2-V supply. The chip performance achieves S_{11} below -10 dB across the entire band and a minimum noise figure of 2.55 dB. The simulated third-order input intercept point is -2.7 dBm. The voltage gain reaches a peak of 11.2 dB in-band with an upper 3-dB frequency of 3.8 GHz, which can be extended to reach 6.2 GHz using shunt inductive peaking. A figure of merit is devised to compare the proposed designs to recently published wideband CMOS LNAs.

Index Terms—Figure of merit (FOM), inductive peaking, low-noise amplifier (LNA), noise figure (NF), wideband amplifiers.

I. INTRODUCTION

WORLDWIDE interoperability for microwave access (WiMAX) is a new wireless technology that provides the high speed of broadband service and broad coverage of up to 70 km in line-of-sight (LOS) environments. The first released active standard of WiMAX, i.e., IEEE 802.16-2004 [1], addressed LOS environments at high-frequency bands operating in the 10–66-GHz range and non-LOS environments in the band between 2 and 11 GHz. Looking forward, IEEE 802.16e adds mobility and enables applications on notebooks and personal digital assistants in the frequency range of 2–6 GHz within three bands, namely, 1) 2.5–2.9 GHz, 2) 3.4–3.6 GHz, and 3) 5.2–5.9 GHz. Wideband low-noise amplifiers (LNAs) help achieve lower power solutions for mobile user equipment through sharing the frontends of multiple bands.

This brief considers the design of a wideband LNA in 0.13- μm CMOS technology for a WiMAX receiver. We present two designs. The first is an inductorless LNA operating in the frequency band between 0.2 and 3.8 GHz to cover the first two WiMAX bands. Its low power consumption as well as its compact size, being inductorless, allow portability and make it suitable for the rapidly evolving IEEE 802.16e standard. The second design uses shunt inductive peaking along with the load capacitance to achieve a bandwidth up to 6.2 GHz to cover the three bands.

II. WIDEBAND CMOS LNAs

Wideband LNAs were reported in CMOS using various topologies. Some used resistive feedback [2]–[4], whereas

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others implemented the LNA using distributed amplifiers [5] that can achieve a very wide bandwidth. Both solutions are power hungry. Other implementations used inductive source degeneration common source LNA with either resistive feedback [6] or using an LC -bandpass filter at the input to achieve wideband matching [7]–[9]. Both techniques used a large number of bulky inductors.

The common gate (CG) LNA topology can be used as a wideband LNA if the inductor used to provide the dc current path as well as tuning out the input capacitance at the required frequency of interest is replaced by a current source [10]. Its main drawback is a relatively high noise figure (NF). Ignoring the noise contribution due to the load, the CG stage has a minimum noise factor given by [11]

$$F = 1 + \gamma \quad (1)$$

where γ is the excess channel thermal noise coefficient.

Some noise cancellation techniques were used to lower the NF of CG LNAs [11]–[13]. A balanced narrowband CG LNA with capacitive cross-coupling technique is used in [11] and [12]. More recently, in [13], a single-ended input differential output wideband LNA is realized using a CG and common source stages in parallel where the wideband matching is achieved using, again, a bulky LC ladder filter at the input with shunt inductive peaking with the load capacitance to widen the bandwidth.

A complete noise analysis of the capacitive cross-coupling transistor is discussed in Section III. A new topology based on capacitive cross-coupling is presented and analyzed. It is shown to achieve a lower NF with lower power consumption and eliminates the bulky inductors used in the original topology [11]. The discussion of the proposed circuit is extended in Section IV. Section V presents the simulation results followed by the conclusions in Section VI.

III. CAPACITIVE CROSS-COUPLING

The capacitive cross-coupling transistor is shown in Fig. 1 [11]. In this circuit, the differential input impedance is given by

$$R_{in} = 2 \cdot (1/2g_{m1}) = 1/g_{m1} \quad (2)$$

where g_{m1} is the transconductance of transistors M1 and M2.

Assume that the dominant sources of noise come from the transistors' thermal noise, then we can analyze the circuit using the simplified model in Fig. 2. Capacitors C1 and C2 are replaced by short circuits since they are much larger than the capacitance of the input transistors. Each inductor is replaced

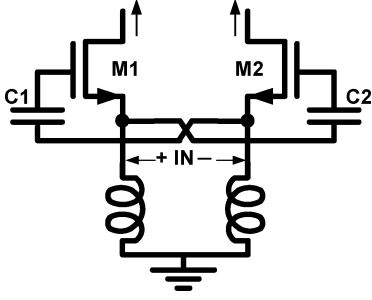


Fig. 1. Capacitive cross-coupling technique.

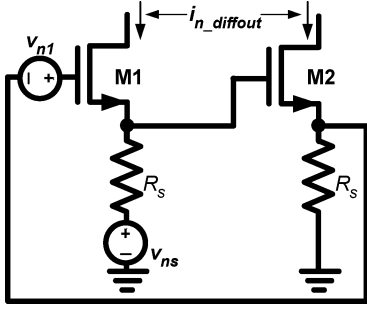


Fig. 2. Simplified form of the capacitive cross-coupling LNA configuration for NF calculation.

by an open circuit because it tunes out the input capacitance in the frequency band of interest. The noise analysis is given as follows: Each half circuit contributes two sources of noise v_{ns} and v_{n1} . v_{ns} creates two equal but opposite currents in the two output branches with absolute value $g_{m1}v_{ns}/2$, giving a differential output noise current of $g_{m1}v_{ns}$, whereas v_{n1} induces two unequal currents in the two output branches but in the same direction so its induced differential output noise current is only $g_{m1}v_{n1}/2$. Therefore, transistor noise partially cancels. The output differential noise current square due to each of the two noise sources is given by

$$\begin{aligned} i_{ns_diffout}^2 &= g_{m1}^2 v_{ns}^2 = 4KT R_s g_{m1}^2 \\ i_{n1_diffout}^2 &= \frac{g_{m1}^2}{4} v_{n1}^2 = 4KT \gamma \frac{g_{m1}}{4} \end{aligned} \quad (3)$$

where the noise factor F is given by

$$F = 1 + \frac{\gamma}{4g_{m1}R_s}. \quad (4)$$

Under the power-matching condition

$$R_s = R_{in}/2 = 1/2g_{m1} \quad (5)$$

then (4) reduces to

$$F = 1 + \frac{\gamma}{2}. \quad (6)$$

If the inductors are replaced by current sources, the NF increases due to the added noise of these transistors.

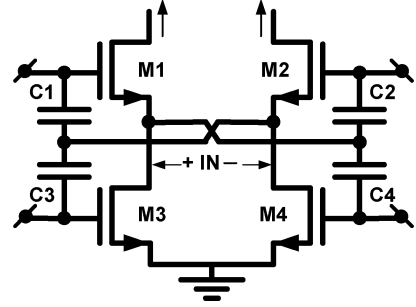


Fig. 3. Proposed dual capacitive cross-coupling technique.

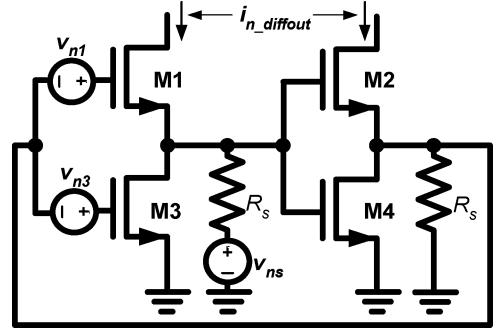


Fig. 4. Simplified form of the dual capacitive cross-coupling LNA configuration for NF calculation.

Our proposed circuit is shown in Fig. 3. Here, M3 and M4 are capacitively coupled. Again, C3 (C_4) needs to be much greater than C_{gs3} (C_{gs4}).

The input impedance is given by

$$R_{in} = 2/(2g_{m1} - g_{m3}) \quad (7)$$

where g_{m1} and g_{m3} are the transconductances of transistors M1 and M3, respectively.

Assuming that the main noise sources are due to transistors' thermal noise, then the circuit is analyzed with the help of Fig. 4, where the capacitors C1–C4 are replaced by short circuits.

The input power-matching condition is given by

$$R_s = R_{in}/2 = 1/(2g_{m1} - g_{m3}). \quad (8)$$

For each half circuit, there are three sources of noise v_{ns} , v_{n1} , and v_{n3} . Using (8), each of v_{ns} and v_{n3} induces equal but oppositely directed currents in the two output branches with absolute values $g_{m1}v_{ns}/2$ and $g_{m1}g_{m2}R_s v_{n3}/2$, respectively. v_{n1} on the other hand induces two unequal currents in the two output branches but in the same direction so its induced differential output noise current is given by $g_{m1}(g_{m1}R_s - 1)v_{n1}$. The output differential noise current square due to each of these noise sources is given by

$$\begin{aligned} i_{ns_diffout}^2 &= g_{m1}^2 v_{ns}^2 = 4KT R_s g_{m1}^2 \\ i_{n1_diffout}^2 &= g_{m1}^2 (g_{m1}R_s - 1)^2 v_{n1}^2 \\ &= 4KT \gamma 1g_{m1} (g_{m1}R_s - 1)^2 \\ i_{n3_diffout}^2 &= g_{m1}^2 g_{m3}^2 R_s^2 v_{n3}^2 = 4KT \gamma 3g_{m1}^2 g_{m3}^2 R_s^2 \end{aligned} \quad (9)$$

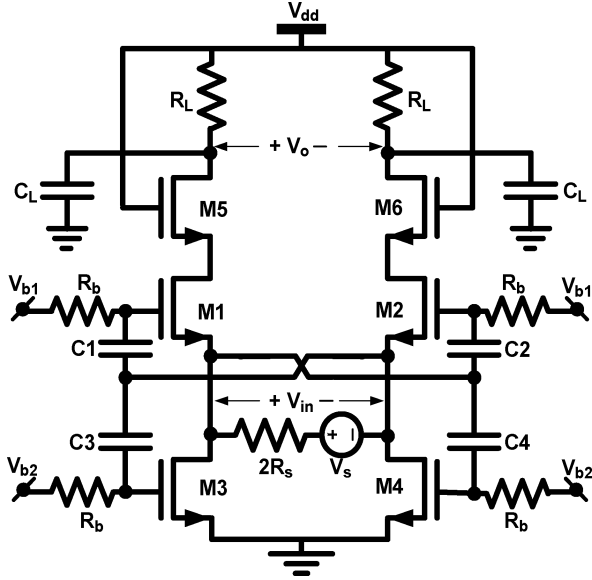


Fig. 5. Core LNA circuit schematic.

where the noise factor F is given by

$$F = 1 + \frac{\gamma_1(g_{m1}R_s - 1)^2}{g_{m1}R_s} + \gamma_3g_{m3}R_s. \quad (10)$$

Assuming $\gamma_1 = \gamma_3 = \gamma$ and using (8), F reduces to

$$F = 1 + \gamma \left[\frac{(g_{m1}R_s - 1)^2}{g_{m1}R_s} + 2g_{m1}R_s - 1 \right]. \quad (11)$$

Differentiating (11) with respect to $g_{m1}R_s$ and equating the result to zero to get the optimum value for $g_{m1}R_s$ for minimum F yields

$$(g_{m1}R_s)_{\text{opt}} = 1/\sqrt{3} \quad (12)$$

for $R_{\text{in}} = 100 \Omega$, $R_s = 50 \Omega$, $g_{m1} = 11.55 \text{ mS}$, and $g_{m3} = 3.1 \text{ mS}$. M3 and M4 contribute exactly half the output noise of M1 and M2, and the minimum noise factor is given by

$$F_{\text{min}} = 1 + \gamma[2\sqrt{3} - 3] = 1 + 0.464\gamma. \quad (13)$$

Therefore, the proposed topology achieves a lower NF than that of the topology in Fig. 1 with the additional advantage of removing the bulky inductors.

IV. WIDEBAND LNA IMPLEMENTATION

The core LNA circuit schematic is shown in Fig. 5 without the biasing circuit required to supply V_{b1} and V_{b2} . M5 and M6 are added for reverse isolation and are of small size to preserve the amplifier bandwidth. M3 and M4 can be coupled without the use of C3 and C4, but in this case, a large dc overhead on M3 and M4 limits the linearity.

M3 and M4 are biased from the same biasing circuit supplying M1 and M2 through high-resistivity polyresistors R_b s

without much excess current consumption. The bias circuit implemented in this brief is similar to that in [11].

The voltage gain ratio V_o/V_{in} is given by

$$\begin{aligned} \frac{V_o}{V_{\text{in}}} &= \frac{(2g_{m1} + g_{ds1}) \cdot (g_{m5} + g_{ds5})}{A_2s^2 + A_1s + A_0}, \\ A_0 &= g_L(g_{m5} + g_{ds5}) + g_{ds1}(g_L + g_{ds5}) \\ A_1 &= C_{d5}(g_{m5} + g_{ds5} + g_{ds1}) + C_{d1}(g_{ds5} + g_L) \\ A_2 &= C_{d1}C_{d5} \end{aligned} \quad (14)$$

where g_{ds1} and g_{ds5} are the output conductances of M1 and M5, respectively, C_{d1} and C_{d5} are the total capacitances at the drains of M1 and M5, respectively, g_{m5} is the transconductance of M5, and g_L is the load conductance.

Neglecting the s^2 term in the denominator and the second term in A_0 , the voltage gain in (14) can be approximated by

$$\frac{V_o}{V_{\text{in}}} \cong \frac{(2g_{m1} + g_{ds1})R_L}{1 + s \left[\frac{C_{d5}(g_{m5} + g_{ds5} + g_{ds1}) + C_{d1}(g_{ds5} + g_L)}{g_L(g_{m5} + g_{ds5})} \right]} \quad (15)$$

which can be further approximated by

$$\frac{V_o}{V_{\text{in}}} \cong \frac{2g_{m1}R_L}{1 + sC_{d5}R_L}. \quad (16)$$

This indicates a midband gain of approximately $2g_{m1}R_L$, which is the same approximated expression if M3 and M4 are replaced by inductors as in [11] and [12]. In our design, a slightly higher gain is achieved due to the higher g_{m1} (11.55 mS compared to 10 mS) without excess current consumption since the biasing current is set by g_{m3} (only 3.1 mS), which results in lower power consumption compared to that reported in [11] and [12].

From (16), we can deduce that the dominant pole in determining the 3-dB bandwidth is the one at the output node where a load capacitance C_L of 90 fF is added in our simulations to model the input capacitance of a succeeding mixer implemented in the 0.13- μm process [13].

V. SIMULATION RESULTS

In this section, we present the simulation results of two LNA designs. The first is inductorless and the other employs shunt inductive peaking with the load capacitance to widen the bandwidth. Both designs use the same transistor, yet, in the case of inductive peaking, a lower load resistor value is used to obtain a reasonable value of on-chip inductance without much degradation in the passband voltage gain.

Fig. 6 shows the simulated NF and input reflection coefficient S11 of the two LNAs plotted versus RF input frequency up to 8 GHz. The minimum NF is 2.55 dB for the inductorless design and 2.62 dB for the design using inductive peaking. Both designs have NF below 2.85 dB across the whole bandwidth, i.e., 0.2–3.8 GHz for the inductorless design and 0.2–6.2 GHz for the other. S11 is below -10 dB up to 7.8 GHz for the two designs.

Fig. 7 shows the amplifier total voltage gain (V_o/V_s) at 11.2 dB in the passband with an upper 3-dB frequency of 3.8 GHz for the inductorless design, whereas it is 10.5 dB with an upper 3-dB frequency of 6.2 GHz when using inductive peaking. The

TABLE I
COMPARISON OF WIDEBAND CMOS LNAs: THIS PAPER AND RECENTLY PUBLISHED PAPERS

Ref. – Year	Technology	Topology	BW (GHz)	NFmin (dB)	NFmax (dB)	S11 (dB)	Gain (dB)	IIP3 (dBm)	Power (mW)	No. of Coils	FOM
[2] – 2004	0.25µm	Feedback	0.02 ~ 1.6	1.9	2.4	<-8	13.7	0	35	0	0.34
[3] – 2003 ^a	0.18µm	Feedback	3 ~ 7	1.4	1.9	<-10	15.3	N/A	15	4	N/A
[4] – 2003	0.18µm	Feedback ^{Diff}	1 ~ 7	3.3	5.5	<-7.2	13.1	-4.7	75	4	0.07
[5] – 2003	0.18µm	Distributed	0.5 ~ 14	3.4	5.4	<-11	10.6	N/A	52	8	N/A
[6] – 2005	0.18µm	Feedback	2 ~ 4.6	2.3	5.2	<-9	9.8	-7	12.6	3	0.093
[7] – 2004	0.18µm ^{Std}	LC-filter based	2.3 ~ 9.2	4	5.2 ^{Average}	<-9.9	9.3	-6.7	9	5	0.21
[7] – 2004	0.18µm ^{TW}	LC-filter based	2.4 ~ 9.5	4.2	5.3 ^{Average}	<-9.4	10.4	-8.8	9	5	0.14
[8] – 2005 ^a	0.18µm	LC-filter based	1.5 ~ 2.6	N/A	0.9	<-10	15.4	-2.5	11	4	1.44 ^c
[8] – 2005 ^a	0.18µm	LC-filter based	3.2 ~ 4.8	N/A	1.6	<-10	17.9	-4.5	13.2	4	0.76 ^c
[9] – 2005 ^a	0.13µm	LC-filter based	3 ~ 10.7	2.2	3 ^{Average}	<-10	11	-8.2	4.8	5	0.87
[10] – 2004 ^a	0.18µm	Common Gate	3.1 ~ 6.1	3.9	4.3	<-12.9	17	N/A	21	3	N/A
[13] – 2005	0.13µm	CG parallel CS ^b	0.1 ~ 6.5	3	4.2	<-10	19	1	11.7	4	4.75
This work ^a	0.13µm	Proposed ^{Diff}	0.2 ~ 3.8	2.55	2.85	<-10	11.2	-2.7	1.9	0	4.29
This work ^a	0.13µm	Proposed ^{Diff}	0.2 ~ 6.2	2.62	2.85	<-10	10.5	-2.7	1.9	2	6.48

a. Simulation results, b. Single ended input differential output c. Maximum noise figure is used to calculate FOM, Diff: Differential, Average: Average noise figure, Std: Standard devices, TW: Twin well devices

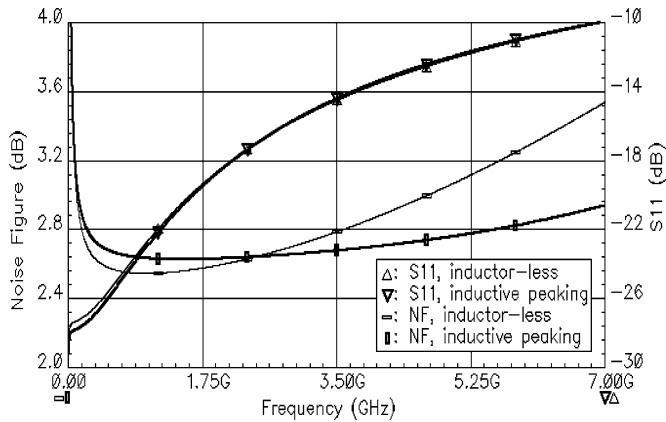


Fig. 6. NF and S11 plotted versus RF input frequency.

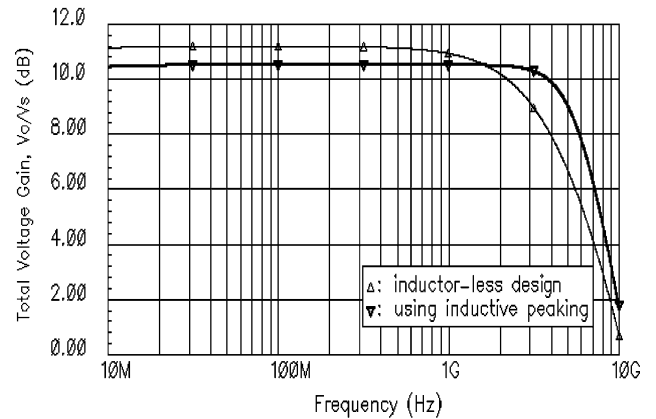


Fig. 7. Total voltage gain (V_o/V_s).

third-order input intercept point (IIP3) for the two designs varies from -2.5 to -2.7 dBm along the bandwidth. Fig. 8 shows an IIP3 of -2.7 dBm when two input tones at 3 and 3.02 GHz are applied simultaneously to the inductively peaked design.

A figure of merit (FOM) is used to compare between the proposed designs and recently published wideband CMOS LNAs. This FOM was originally proposed in [14] and used in [15] for narrowband LNAs and is modified here to suit wideband LNAs by replacing the center frequency term by the 3-dB bandwidth, i.e.,

$$FOM = \frac{Gain [absolute values] \cdot IIP3 [in milliwatts]}{P_{dc} [in milliwatts] \cdot (F - 1) [absolute values] \cdot BW [in gigahertz]}. \quad (17)$$

Table I compares the FOM of recent publications to ours. The gain used is the total voltage gain (V_o/V_s), which equals the power gain in the designs having input and output impedance matching. The power consumption used is that consumed in the LNA core only. In some designs, the average NF within the band is reported so it will be the one used in the FOM. In the designs having only maximum and minimum NFs within the band reported, their arithmetic average is calculated and used.

VI. CONCLUSION

The design of an inductorless wideband LNA for WiMAX is introduced. It achieves a minimum NF of only 2.55 dB with a total voltage gain of 11.2 dB. The amplifier achieves good power matching and linearity from 0.2 to 3.8 GHz with very low power consumption. Shunt inductive peaking extends the

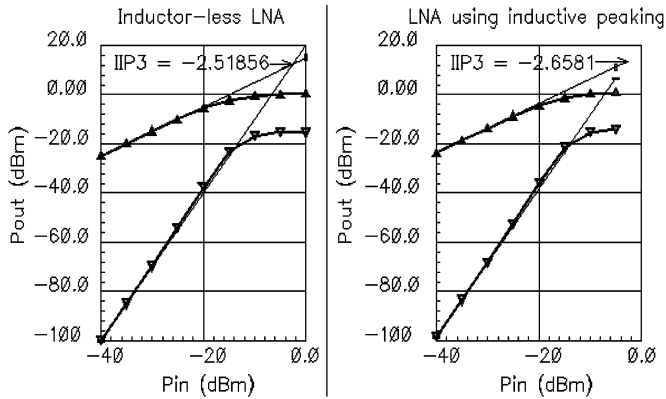


Fig. 8. Input-referred IIP3.

LNA bandwidth up to 6.2 GHz with 10.5-dB total voltage gain. For both designs, the core LNA consumes only 1.9 mW from a 1.2-V supply, whereas the biasing circuit consumes 0.33 mW.

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